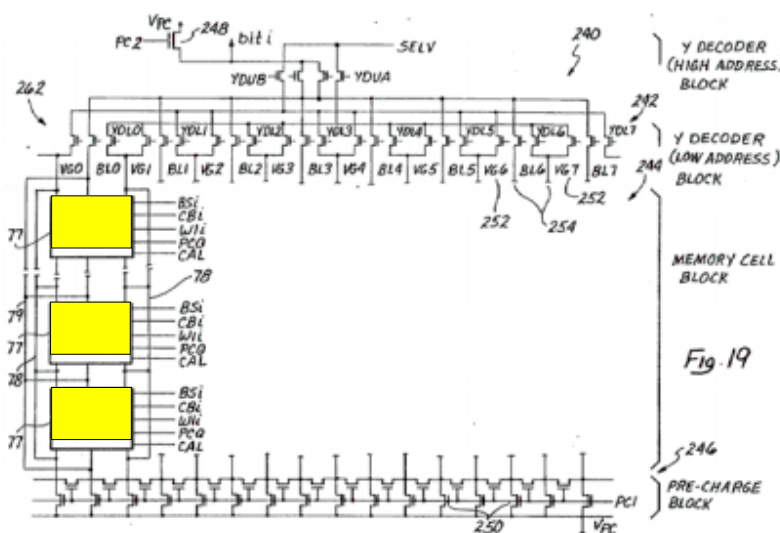


VARIOUS EMBODIMENTS OF THE INVENTION MUST BE WELL SUPPORTED IN THE SPECIFICATION, DRAWINGS, AND PROSECUTION HISTORY TO BROADEN THE SCOPE OF THE CLAIMS

By: Mel R. Quintos

Decided on June 3, 2013, the U.S. Court of Appeals for the Federal Circuit (CAFC) case of *Creative Integrated Systems, Inc. v. Nintendo of America, Inc.* is an appeal by plaintiff Creative Integrated Systems after a *Markman* hearing where claim language is interpreted. The district court found that Nintendo of America did not infringe Creative Integrated Systems' improved ROM (read only memory) device.

The patent at issue, U.S. Patent No. 5,241,497, relates to improvements in the circuitry and methodology of the sub-circuits included within a very large scale integrated (VLSI) ROM. Illustrated below is the memory cell array that contains all of the data stored in the ROM. Three lines connect the cell blocks 77 to one another with the following metallization lines: a ground line VG0, a ground line VG1, and one main bit line BL0.



Claim 12, a representative claim at issue, states that “the plurality of blocks [are] coupled together at their ends by metallization lines.”

The issue before the CAFC is whether claim 12 is to be interpreted based on a memory cell block within a memory cell array that embodies Figure 7 or a memory cell block that embodies Figure 9 (please see back page). In other words, did the district court make an error in interpreting the relevant claim based solely on the memory cell block of Figure 7?

A claim interpretation based on the embodiment of Figure 7 results in a finding of non-infringement by Nintendo of America, while a claim interpretation based on the embodiment of Figure 9 provides an opposite result of infringement by Nintendo of America in favor of the patent owner, Creative Integrated Systems.

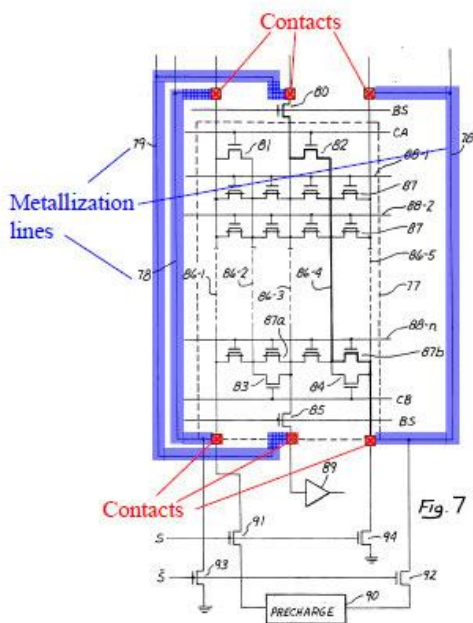


FIGURE 7 (No Infringement)

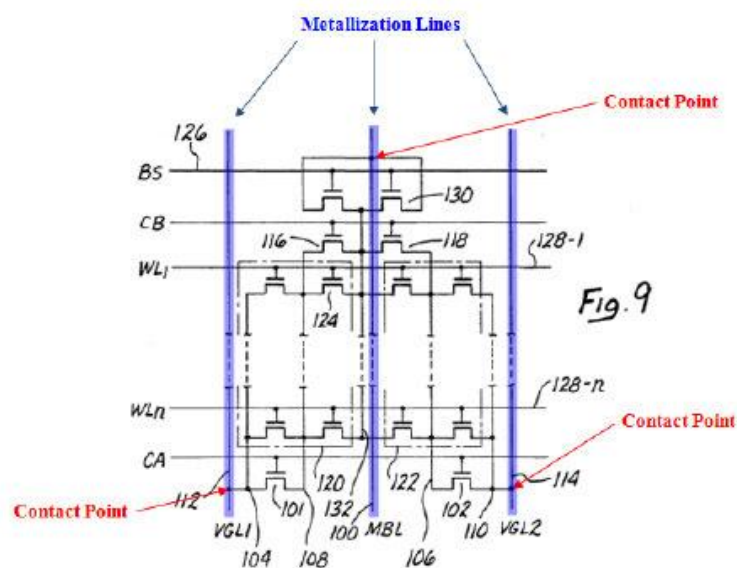


FIGURE 9 (Infringement)

Both embodiments perform similar functions by enabling a block select line BS to connect the block to the main bit line MBL. The desired bit within the block is designated by selectively enabling the word lines WL in that block to create a path from one of the ground lines to the main bit line where the bit may be read. The Figure 7 embodiment employs six contact points, while the Figure 9 embodiment requires only three contact points (i.e., one in the middle for the main bit line MBL, and two on the sides for the ground lines VGL).

In interpreting claim 12, the CAFC ruled that the district court correctly determined that the plain language of claim 12 did not restrict the metallization lines to connect to each end of each block, and therefore, claim 12 is not restricted to the Figure 7 embodiment. However, based on the specification and prosecution history, the district court was wrong in interpreting claim 12 based only on the structure of Figure 7 because: (1) “[t]he specification and drawings in this case describe over a dozen improvements to various components of ROM circuitry . . . described by the figure 7 and figure 9 embodiments,” and (2) during the prosecution history, there were some amendments and arguments that clearly expressed “that each end of an individual block is connected to the other [Figure 7 embodiment],” and some directed to claim limitations “requiring only that the metallization lines connect one block to the next [Figure 9 embodiment].”

Decision: The district court’s claim interpretation restricting the metallization lines to connect to contacts at each end of each block (only Figure 7 embodiment) is erroneous, and is REVERSED. The district court’s finding of non-infringement is therefore VACATED.

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